WHITE PAPER

Successful Carrier Card Design for COM Express™: Introduction to High Speed Serial Bus Interface Design

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While the COM Express standard offers a number of advantages for embedded system design, designers must also consider some of the potentially new issues they face when designing carrier cards for the modules. Besides physical features (component height), designers need to consider several electrical features—impedance matching, termination, and noise susceptibility—and EEPROM interfacing. When designing specific busses, designers must also consider bus-specific criteria and this white paper gives several examples.

THE NEXT GENERATION COMPUTER-ON-MODULE STANDARD

COM Express is a modular embedded computing solution. It provides the answer for applications requiring higher CPU performance options, higher I/O bandwidth, and design flexibility in an extremely compact form. Ratified in July 2005 by the PCI Industrial Computer Manufacturers Group (PICMG), the COM Express standard defines the mechanical, electrical and thermal requirements for a highly integrated COM mezzanine. The standard specifies a rich set of high-speed serial I/O interfaces and provides the option to preserve key current parallel interface technologies to ensure a smooth migration path.

The standard offers the obvious benefits of standardization and modularity. In addition, it also enables broader design reuse, reduced development expense and significantly less risk. This gives designers faster time-to-market and time-to-revenue. Potential markets for COM Express include medical, test and measurement, gaming, entertainment, industrial automation and point-of-sale among others.

The specification defines two module sizes. The basic module is 95 mm × 125 mm, and the larger, pin compatible extended size is 110 mm × 155 mm. Both support internal and external graphics, multiple display devices, audio, networking, storage and various I/O and of course PCI Express interfaces, the core of the I/O structure. The bigger module supports both higher performance processors and larger capacity memory designs.

The specification defines no cables or external connectors. All interfaces between the module and carrier card are through the 440-pins of the two mezzanine connectors. Figure 1 illustrates the basic features of a typical COM Express Module.

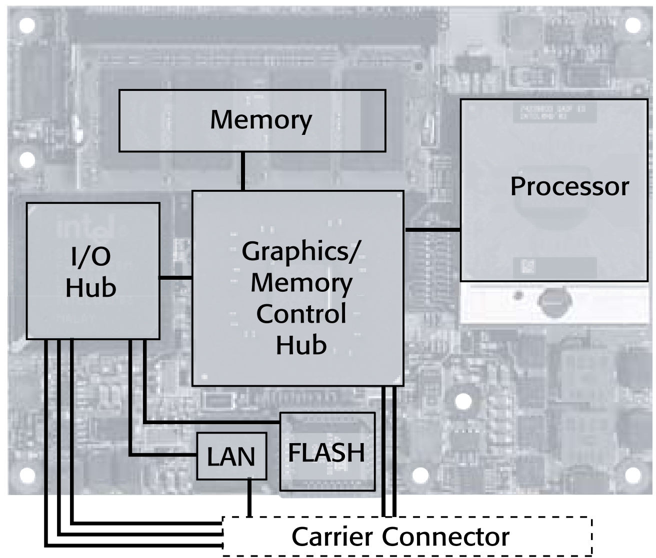

Figure 1 Typical COM Express Module ©PICMG 2005

DESIGNING HIGH SPEED SERIAL BUS INTERFACES

Several companies will manufacture and market computer system modules that developers can design application-specific carrier cards of any size and shape for. Regardless of the carrier card design, there are a few similar considerations for every design.

- Physical and mechanical (especially component height)
- Electrical (impedance matching, termination, noise and transmission line loss)
- Carrier card to module control interfacing

For the purposes of example, we are using RadiSys modules as examples throughout this white paper.

MECHANICAL PLACEMENT AND COMPONENT HEIGHT

The COM Express specification states that the components mounted on the backside of the module in the space between the bottom surface of the module PCB and the carrier card must have a maximum height of 3.8 mm (DIM B in Figure 2.)

There are two carrier card stack options: 5 mm and 8 mm, which require the use of different connectors.

With the 5 mm stack option, the clearance between the carrier card and the bottom surface of the module's PCB is 5 mm (DIM A). The specification states that components placed on the carrier card topside under the module envelope are limited to a maximum height of 1 mm (DIM C) with the exception of the mating connectors. Using carrier card topside components up to 1 mm allows a gap of 0.2 mm between carrier-card module bottom-side components. However, this may not be sufficient space in some situations, for example where flex or severe vibration are expected.

If you design a carrier card using the 8 mm stack option, then the carrier card topside components within the module envelope are limited to a height of 4 mm (DIM C) with the exception of the mating connectors. Using carrier card topside components up to 4 mm again allows a gap of 0.2 mm between carrier card topside components and module bottom side components. However, a larger gap may be easily created by using a lower component height envelope that the one specified in the standard.

Carrier cards intended only for use with pin-out Type 1 modules may use a single 220-pin, 0.5 mm pitch receptacle.

The carrier card connector for module pin-out Types 2 through 5 must use a 440-pin plug that is composed of two pieces of a 220-pin, 0.5 mm pitch plug. (The connector pair can be held together by a plastic carrier during assembly to allow handling by automated assembly equipment.)

The connectors need to be qualified for low voltage differential signaling (LVDS) operation up to 6.25GHz for support of PCI Express Generation 2 signaling speeds.

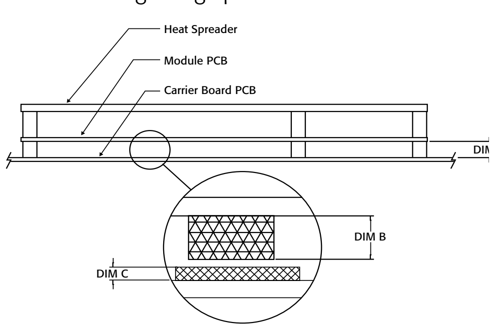

Figure 2. If parts are mounted on the top of the carrier card (DIM C) the component height is the physical dimension of most concern in carrier card design. ©PICMG 2005

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ELECTRICAL CONSIDERATIONS

Regardless of the bus, basic electrical considerations for carrier card developers include impedance matching and ground referencing for the differential pairs, signal termination and noise susceptibility.

- ***Impedance Matching –*** All signal references are normally to ground and traces should run over continuous ground planes.
- ***Termination –*** Usually the transmission pairs require termination if not used. (USB signals require no termination.)
- ***Noise Susceptibility –*** Route differential pair traces away from any large noise generating devices such as crystals, oscillators and clock drivers, because noise will affect the signals transmitted.
- ***Transmission Line Loss –*** Calculate the sum of the transmission line losses (or loss budget) caused by modules, cards, connectors and cables. This will ensure that the trace lengths on the carrier card, and their associated losses, are kept short or small enough to keep the overall losses within limits of the bus specification.

CARRIER CARD EEPROM INTERFACING CONSIDERATIONS

The EEPROM allows the COM Express module BIOS to set up any software configurable module features that are appropriate for the carrier card, this includes the PCI Express link configuration. If there is an incompatibility between the expected carrier card configuration and the module capabilities, an error message may be generated. Error messaging is not defined by the standard and is vendor-module specific.

As defined in the specification, the EEPROM may also describe the expected link presence for SATA (serial advanced technology attachment), Express Card, USB, TV-Out, VGA, LVDS (low voltage differential signaling), SDVO (serialized digital video output), LAN, audio, and the expected presence of miscellaneous I/O signals.

HIGH SPEED SERIAL BUS INTERFACE DESIGN EXAMPLES:

In all examples that follow, trace spacing and dimension information is based on RadiSys carrier-card design and is for your reference only. The correct trace width and spacing for the correct impedance's can only be calculated after the PCB stackup is known. (For more details, please see the design guide mentioned in references below.)

PCI EXPRESS GUIDELINES

PCI Express uses some terms that are used to define the logical and physical configurations of the bus, to provide the required signal paths, of appropriate bandwidth, between devices.

- ***Lane*** (or PCI Express lane) is a set of four pins on the COM Express connector that can be used for a single PCI Express transmit pair and a single receive pair. Clocking information is embedded into the data stream.
- ***Link*** (or PCI Express link) is a group of PCI Express lanes between two PCI Express agents. Allowable link widths are ×1, ×2, ×4, ×8, ×16 and ×32. An ×1 link utilizes 1 lane; an ×2 link 2 lanes; etc. The link bandwidth scales up proportionally with the link width.
- ***Bucket*** (or PCI Express bucket) is a group of PCI Express lanes on the COM Express connector. The 32 PCI Express lanes on the COM Express connector are conceptually divided into buckets to facilitate a description of how the available PCI Express lanes should be assigned to COM Express connector pins. A bucket is not a link. The term is simply a conceptual vehicle to facilitate the description of an orderly mapping of chipset PCI Express lanes to COM Express connector PCI Express lanes.

PCI EXPRESS LINK CONFIGURATION

The COM Express module allows you to configure up to a maximum of 32 PCI Express lanes for use, which gives the equivalent bandwidth of 4×10G Ethernet connections! However, the count varies with the module pin-out type.

Chipsets on COM Express modules have a variety of PCI Express lane and link capabilities. On some chipsets, the PCI Express lanes can be grouped into various links under software control, while on other chipsets, the PCI Express links are of a fixed width. The mapping of the chipset PCI Express lanes to the COM Express lanes and the grouping of the lanes into links is referred to as *link configuration*. Figure 3 diagrams the types of possible link configurations available.

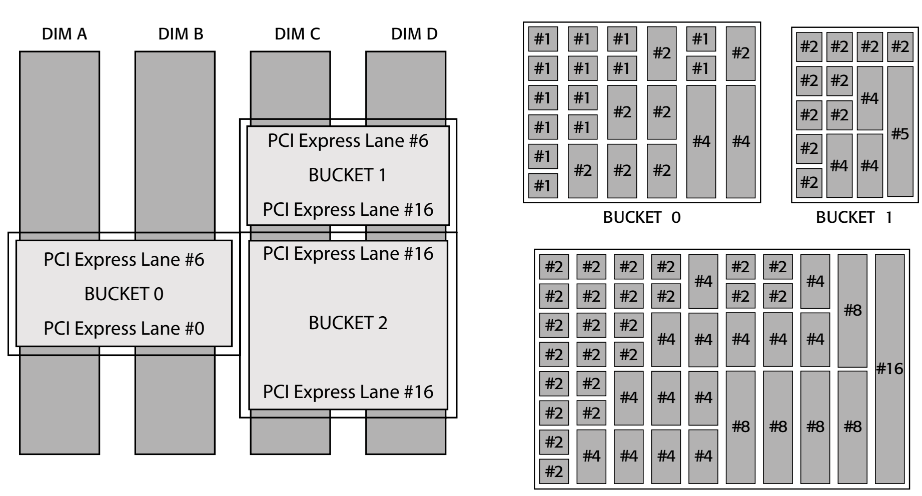

Figure 3. Sample PCI Express link configurations show how buckets define many possible link configurations. ©PICMG 2005

DESIGN CONSIDERATIONS

There are four main design considerations that designers should consider for PCI Express carrier cards:

- Reference all PCI-Express signals to ground and route all traces over continuous ground planes.
- Route transmit-and-receive PCI Express lanes as differential pairs and keep the differential impedance within the range of 100 ohms ±20%. Each trace of the differential pairs should have the same length, the same number of vias (layer changes in the PCB) and be in the same relative position.
- When changing layers, ensure trace matching for either transmit or receive pair in the same layer and a grounded via should be placed within 250 mils of the layer changed point.
- Avoid routing PCI-Express traces under crystals, oscillators, clock drivers and similar noise generating devices, because noise will affect the signals transmitted.

Table 1: PCI Express Specifications	Definition
Topology	Differential pair point-to-point with serial AC capacitor
Reference plane	Ground reference
Differential mode impedance	100 ohm ±20%
Nominal trace width	4.75 mils
Nominal pair spacing	5.75 mils
Differential pair trace length mismatching	Max = 5 mils
Pair-to-pair spacing	Min = 20 mils
Spacing to other signals	Min = 20 mils
Total trace length on carrier card	Min 0 mils; max 15 inches

Figure 4 and Table 2 describe how to calculate the overall insertion loss budget for the module, carrier card with a PCI-Express card connector, a slot card and their connectors ($L_A+L_B+L_C+L_D+L_E$) to stay within the specified limit.

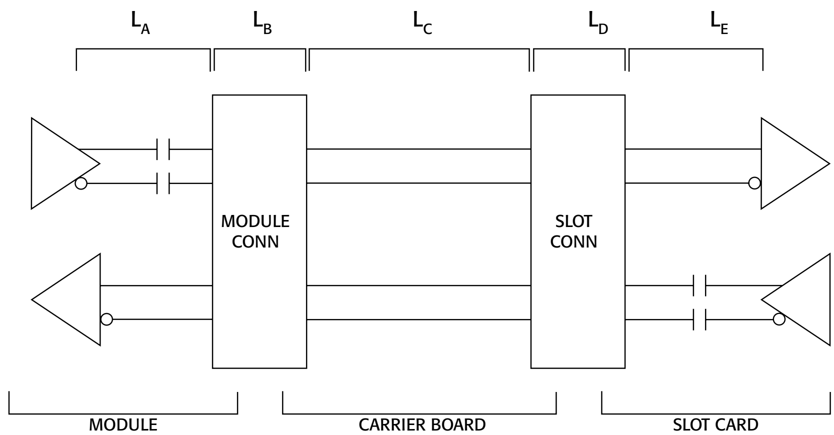

*Figure 4. PCI Express insertion loss budget includes the module, carrier card, slot card and connectors (*sum of = $L_A+L_B+L_C+L_D+L_E$*). ©PICMG 2005*

Table 2: PCI Express Segment Losses (See Figure 4.)		Definition
L_A	3.46	Allowance for 5.15 inches of module trace @ 0.28 dB/GHz/Inch and 1.66 dB crosstalk allowance. Coupling caps not included.
Coupling Caps	1.19	From PCI Express Card Electromechanical Spec Rev. 1.1, parameters (L_{ST} - L_{SR}). Includes crosstalk allowance of 0.79 dB.
L_B	0.25	COM Express™ connector at 1.25 GHz measured value.
L_C	4.40	Allowance for 9 inches of Carrier Board trace @ 0.28 dB/GHz/inch and a 1.25 dB crosstalk allowance.
L_D	1.25	PCI Express Card Electromechanical Spec Rev 1.1 “guard band” allowance for slot connector – includes 1.0 dB connector loss
L_E	2.65	From PCI Express Card Electromechanical Spec, Rev 1.1 (without coupling caps; L_{AR}.) Implied crosstalk allowance is 1.25 dB.
Total	13.20	

Figure 5 and Table 3 explain how to calculate the overall insertion loss budget for the module, carrier card with only on board PCI-Express lanes (L_A+L_B+L_C) to stay within the specified limit.

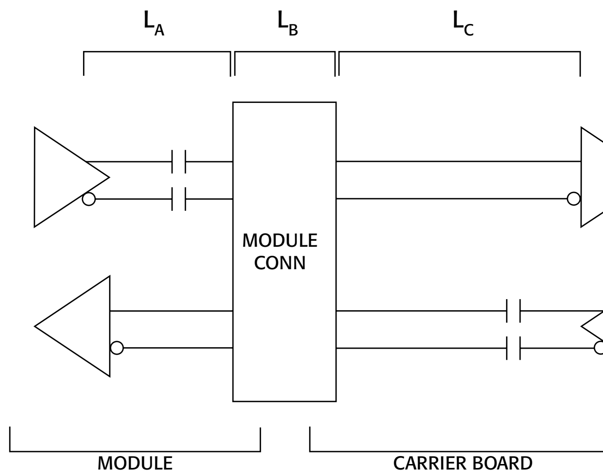

Figure 5. PCI Express insertion loss budget with carrier card PCIE device involves the module, the module connector and the carrier card equals the sum of L_A+L_B+L_C. ©PICMG 2005

Table 3: PCI Express Insertion Loss Budget Calculated (See Figure 5).

Segment	Loss (dB)	Notes
L_A	3.46	Allowance for 5.15 inches of module trace @ 0.28 dB/GHz/inch and 1.66 dB crosstalk allowance. Coupling caps not included.
Coupling Caps	1.19	From PCI Express Card Electormechanical Spec., Rev 1.1, parameters (L_{ST} - L_{SR}). Includes crosstalk allowance of 0.79 dB.
L_B	0.25	COM Express™ connector at 1.25 GHz measured value.
L_C	8.30	Allowance for 15.85 inches of Carrier board trace @ 0.28 dB/GHz/ inch and a 2.75 dB crosstalk allowance.
Total	13.20	

SERIAL ADVANCED TECHNOLOGY ATTACHMENT (SATA) GUIDELINES

Consider the following three main design considerations when designing SATA carrier cards:

- All SATA signals must be ground referenced. Route all traces over continuous ground planes, with no interruptions. Avoid crossing an over split-plane.
- Minimize layer changes. Use fewer vias as possible for each SATA trace. If a layer change is necessary, ensure length match for either transmit or receive pair on each layer.
- Keep noise to a minimum by not routing SATA traces under crystals, oscillators, clock drivers and other kind of large noise generating devices.

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Table 4: SATA Specifications

Parameter	Definition
Topology	Differential pair point-to-point with serial AC capacitor
Reference plane	Ground reference
Differential mode impedance	100 ohm ± 20%
Differential pair trace length mismatching	Max = 20 mils
Pair-to-pair spacing	Min = 20 mils
Spacing to other signals	Min = 20 mils
Total length on carrier card	Min 0 mils; max 7 inches

Figure 6 and Table 5 explain the overall insertion loss budget for a SATA applications, includes the module, module connector, carrier card and cable (L_A+L_B+L_C+L_D). Calculate these losses to stay within the required limit.

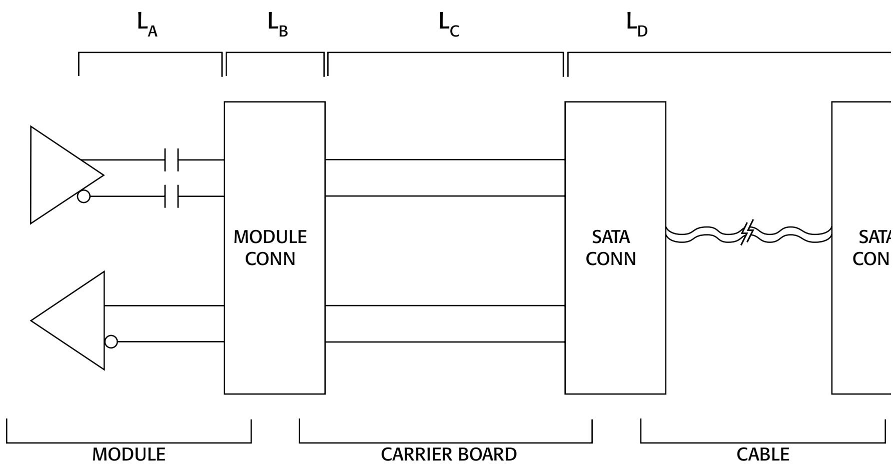

Figure 6. SATA insertion loss budget for the module, carrier card, connectors and cable (sum of L_A+L_B+L_C+L_D). ©PICMG 2005

Table 5: SATA Gen1 (1.5 GHz) and Gen 2 (3.0 GHz) Insertion Loss Budget Calculated

Segment	Loss (dB)	Notes
L_A	Gen 1: 1.26 Gen 2: 1.68	Up to 3.0 inches of module trace at 0.28 dB/Ghz/inch Up to 2.0 inches of module trace at 0.28 dB/GHz/inch
Coupling Caps	Gen 1: 0.40 Gen 2: 0.40	
L_B	Gen 1: 0.25 Gen 2: 0.38	COM Express connector at 1.5 GHz measured value COM Express connector at 3.0GHz measured value
L_C	Gen 1: 3.07 Gen 2: 2.52	Up to 7.2 inches of carrier card trace at 0.28 dB/GHz/inch Up to 3.0 inches of carrier card trace at 0.28 dB/GHz/inch
L_D	Gen 1: 6.0 Gen 2: 6.0	Source specificaion cable and cable connector allowance
Total	Gen 1: 10.98 Gen 2: 10.98	

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VIDEO GUIDELINES

The design considerations for different video options on the carrier cards can vary. These options are for SDVO, LVDS, TV Out and VGA which are explained below.

Consider the following main design considerations when designing carrier cards with video options:

SERIALIZED DIGITAL VIDEO OUTPUT (SDVO)

Consider the following design points when developing

SDVO carrier cards:

- Route the DVI traces on the signal layer adjacent to a continuous ground plane.
- AC coupling capacitors for each channel and are typically installed on the COM module, so no extra capacitors are needed on carrier card for AC coupling.
- COM Express modules support two SDVO interfaces (SDVOB [channel 1] and SDVOC [channel 2]) that share pins with PCI-Express ×16.
- When it's designed to use DVI mode, carrier card must incorporate video CODEC for SDVO interfaces.
- Each SDVO interface is comprised of three differential pairs and associated differential clock. An example device is that can be used for the DVI interface is the Chrontel CH7307.
- When implementing SDVO devices on the carrier card, the SDVO_CLK and SDVO_DATA lines require pull-up resistors to 2.5V ±5%. The value of these resistors should be 3.5K ohms.
- When implementing slots for SDVO carrier cards on the carrier card, there is no need to place the pull-up resistors on the carrier card because add-on SDVO cards already have pull-up resistors.

LOW VOLTAGE DIFFERENTIAL SIGNALING (LVDS)

Consider the following design considerations when creating LVDS carrier cards:

- Route the signal trace as strip line and keep them ground referenced.
- Control differential impedance of the differential pairs within 100 Ohms ±15%
- The differential pairs of the signals must be length matched within 20 mils.
- The LVDS flat panel differential pairs (LVDS_A±, LVDS_B±, LVDS_A_CK±, LVDS_B_CK±) shall have 100 ohm terminations across the pairs at the destination. This may be on the carrier card, if it implements a LVDS de-serializer on-board.
- The two pairs of clocks (LVDS_A_CK±, LVDS_B_CK±) must be length matched within 20 mils.
- Each channel of the LVDS bus must be length matched with the corresponding clocks within 20 mils.
- Minimal space between neighboring traces and differential pairs must be kept over 20 mils.
- Unused LVDS lines may be left open.

TV OUT

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If TV Out is used, the TV_DAC_A, TV_DAC_B, and TV_DAC_C lines must be terminated on the carrier card through a 150 ohm resistor to ground. The termination resistors must be placed close to the external TV-Out connector(s). These lines may be left un-terminated if the TV Out function is not used.

VGA

If analog VGA is used, terminate the VGA_RED, VGA_GRN, and VGA_BLU signals on the carrier card through a 150 ohm resistor to ground. These resistors should be placed close to the VGA connector on the carrier card. However, these lines may be left unterminated when the analog VGA function is not used.

Table 6: Video Specifications

Parameter	Definition
Uncoupled single ended impedance	55 ohms ± 15%
Reference plane	Ground reference
Differential mode impedance	92.6 ohm ± 20%
Differential pair trace length mismatching	Max = 5 mils
Pair-to-pair spacing	Min = 20 mils
Spacing to other signals	Min = 10 mils
Total trace length on carrier card	No more than 15 inches

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USB GUIDELINES

Consider these three main design considerations when developing any USB carrier card:

- USB pairs require no termination. A common mode choke is advisable if USB pairs on the carrier card are routed to a connector for use with an external cable.
- Signals USB_0_1_OC#, USB_2_3_OC#, USB_4_5_OC# and USB_6_7_OC# are used to flag a USB over-current situation.
- Carrier card USB current monitors may pull these lines to ground with open drain drivers to indicate that the monitor's current limit has been exceeded. Do not pull up these lines to 3.3V on the carrier card — this is done on the module.

Figure 7 and Table 7 explain how to calculate the overall insertion loss budget for the module, carrier card, connectors and cable ($L_A+L_B+L_C+L_D+L_E$) to stay within the specified limit.

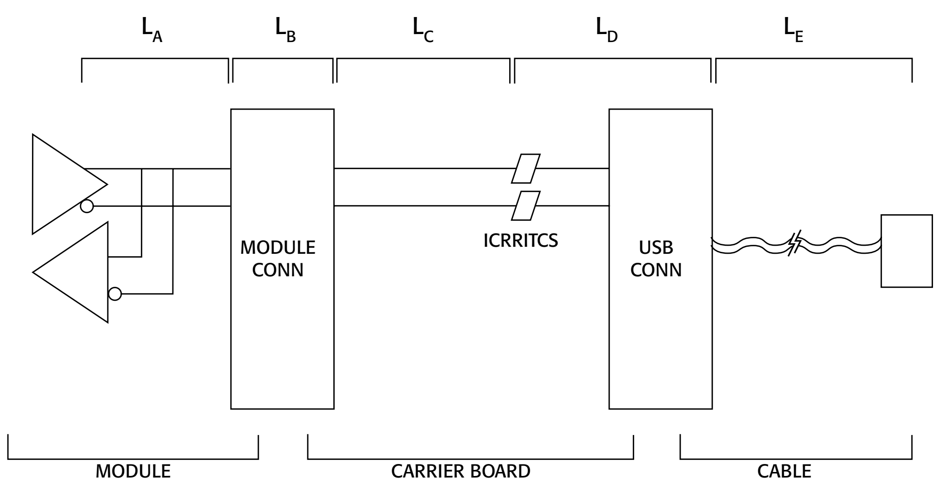

Figure 7. USB insertion loss budget includes module, carrier card and cable (sum of $L_A+L_B+L_C+L_D+L_E$.) ©PICMG 2005

Table 7: USB Loss Budget Calculated

Segment	Loss (dB)	Notes
L_A	0.67	Up to 6 inches of module trace @ 0.28 dB/GHz/inch
L_B	0.05	COM Express™ connector at 400MHz measured value
L_C	1.68	Up to 14 inches of Carrier Board trace @ 0.28 dB/GHz/Inch
L_D	1.00	USB connector and ferrite loss
L_E	5.80	USB cable and far end connector loss, per source specification
Total	9.20	

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CONCLUSION

For manufacturers and developers, decoupling the processor module from the rest of the system designers focuses their attention on developing I/O carrier cards that can address the various applications, product configurations, price points and models specific to their industry. A multiplatform architecture using COM Express for embedded design allows the reuse and interchangeability of modules and/or carriers. It also permits the use of common software libraries, operating system support packages and application middleware. This approach reduces their design risk, cuts development expenses and provides faster time-to-market and time-to-revenue.

The COM Express standard allows OEMs and customers to keep pace with CPU and chipset technology better. Broad industry participation in the standard will enable the competition, rapid innovation and cost reduction that will allow them to keep pace with technology changes.

ABOUT THE AUTHOR

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Andrew Pitt joined RadiSys in 1999 and in his current role develops strategic relationships with customers and provides technical expertise to major accounts in Europe. With more than 20 years in the high tech industry Pitt has held several positions of increased responsibility in sales and technical management. Pitt has special responsibilities for the Procelerant product family and the Commercial markets within the EMEA geography.

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RadiSys COM Express Design Guide [link?]

COM Express: The Next Generation Computer on Module Standard White Paper

RadiSys Webinars on COM Express: www.radisys.com/ce_webinars

GLOSSARY

COM: computer-on-module

DIM: dimension

EEPROM: electrical erasable programmable read-only memory

LVDS: low voltage differential signaling

PCI: peripheral component interconnect

PCIMG: PCI Industrial Computer Manufacturers Group

SATA: serial advanced technology attachment

SDVO: serialized digital video output

SDVOB: SDVO channel 1

SDVOC: SDVO channel 2

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